Remarks / Arguments

Claims 1-4, 6, 10-12, 17, 21, 22 and 26 are amended. Claim 27 is newly added.

I.
Support for Amendments

Support for the amendments may be found throughout the specification and claims. Exemplary support is provided for each amendment.

Claims 1 and 10 are not amended in scope but instead reworded to further clarify that each wafer undergoes wet-chemical treatment and that each top side of the wafer which is not to be treated is always positioned above the liquid. In this regard, the terms "wafers" and "top sides" are amended to singular form. It should now be clear that each wafer undergoes the wet-chemical treatment and the top side of the wafer which is not to be treated is always positioned above the liquid.

Claims 3, 4, 6, 11, 12, 17, 21, 22 and 26 are also amended to recite terms in singular form for consistency with amended claims 1 and 10.

Claim 27 is newly added and provides:

> A process for wet-chemical treatment of electrically conductive edges of a silicon wafer using a liquid bath, during which treatment the silicon wafer lays on conveyor means, wherein the underside and electrically conductive edges to be treated are conveyed through or over etching liquid located in the liquid bath to remove conductivity from the edges, further wherein the conveyor means are positioned within the liquid bath, further wherein an electrically conductive top side of the wafer which is not to be treated is always positioned above the liquid.

Support may be found in claims 1 and 10. Further support may be found at page 2, lines 4-10,

> "One problem with this surface modification is that generally not only the desired surface (top side) but also the opposite surface (underside) and in particular the peripheral edges of the substrate wafers are modified or doped by the treatment, which in subsequent use leads to the risk of short circuits, since the edges are electrically conductive."

Still further support may be found at page 5, lines 5-10,

> "According to one embodiment, it is possible, for example, for just the top side or underside of a corresponding substrate, such as a silicon wafer, to be modified by etching, so that the problem of the formation of short circuits is eliminated in a simple way."

Still further support may be found at page 5, lines 14-19,

> "According to a particularly preferred embodiment, the process according to the invention is carried out as part of a continuous processing, in which undersides of the substrates, such as in particular silicon wafers (if desired including the peripheral edges) are wetted with an etching liquid located in a liquid bath."

Still further support may be found at page 5, line 35 through page 6, line 4,

> "For this purpose, the silicon wafer is oriented substantially horizontally, and the side which is to be etched is wetted with an etching liquid located in a liquid bath. The distance between the etching liquid and the underside of the silicon wafer is selected to be such that the side of the substrate which is to be etched (if desired including the peripheral edges) is wetted, but the opposite side is not."

II.

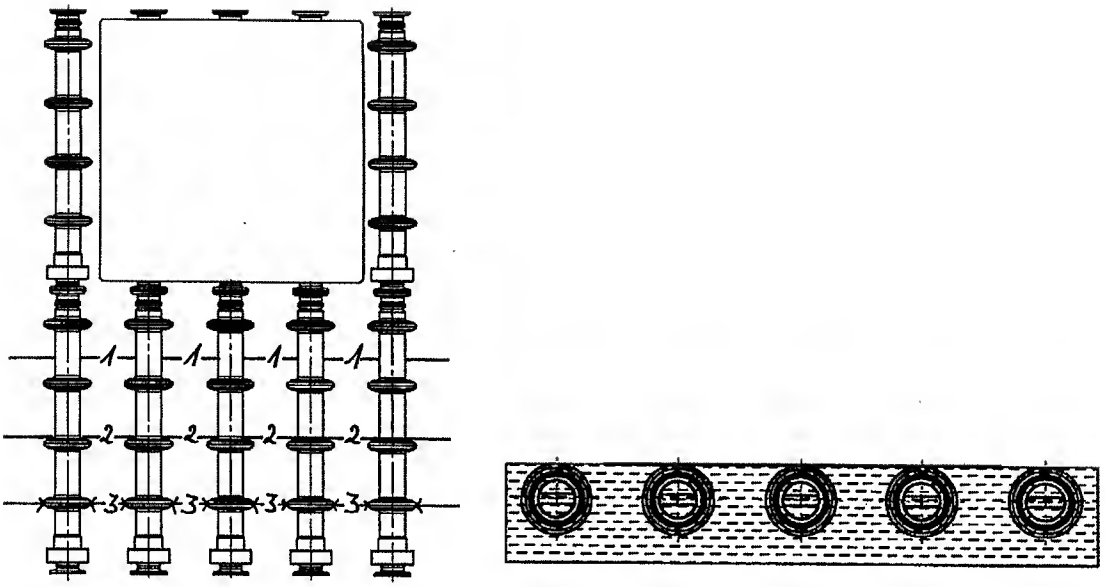
Introduction to the Invention

Claims 1-26 are directed towards methods for treating one side of a silicon wafer. Compared to previous methods, claims 1-26 provide methods that drastically reduce the handling steps involved, which further reduces the risk of breakage of the usually thin and fragile silicon wafer. This is accomplished in part by developing processes that permit the wafer to lay on a conveyor means and be conveyed through or over liquid in a controlled manner, which is only possible when wafers do not float away.

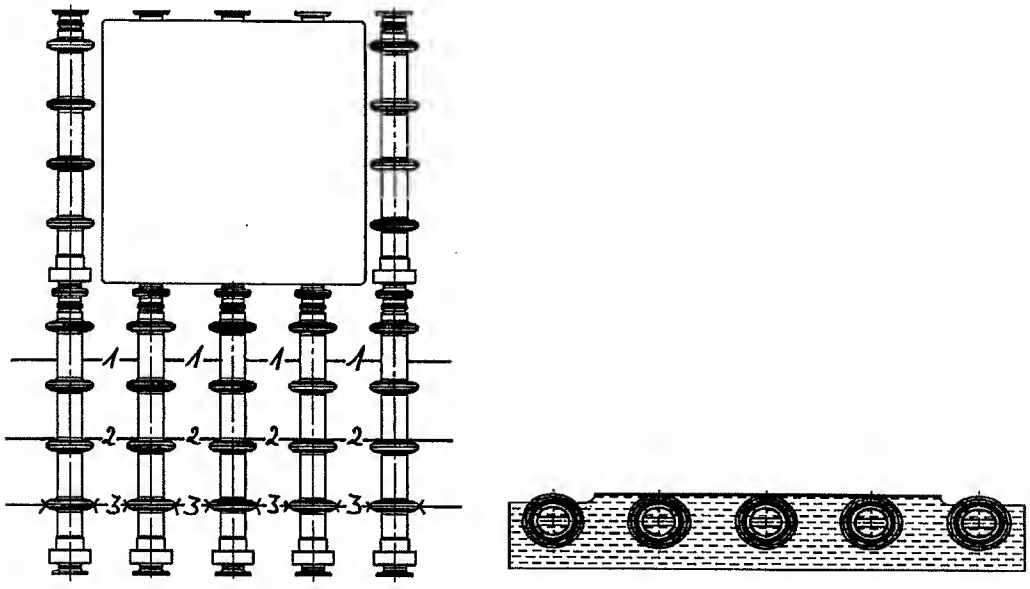
Initially it was expected that any attempt at conveying a wafer through or over liquid would cause the wafer to float away due in part to the high surface area to low weight ratio of the wafer as well as adhesion and cohesive forces and the surface tension of liquids. In other words, once a liquid approaches the level of a conveyor means, it is expected that a wafer will lose contact with the conveyor means and float away from its desired path. This is in contrast to glass substrates, which for instance due to their lower surface area to weight ratio, tend to sink in liquids. That is, silicon wafers tend to float when placed in solution; whereas glass substrates sink.

In this regard, it was surprising to learn that the wafer during treatment can be conveyed through or over the liquid in a controlled and targeted manner without floating apart from a predetermined path.

Now turning to specific claims, claim 1 and claims that depend therefrom provide a process where a silicon wafer is conveyed through or over a liquid located in the bath. In each instance the underside is treated with the liquid; however, the top side is not treated. An example of such a configuration is provided below:



Claim 10 and claims that depend therefrom provide a process where the underside of a silicon wafer is contacted by a liquid in the liquid bath, and the underside is maintained above the level of the bath surface not being contacted by the underside. Again, the top side is always positioned above the level of the liquid. An example of such a configuration is provided below:



Further, applicant newly adds independent claim 27 which provides a method for treating a silicon wafer to remove conductivity from the edges. Conductivity along wafer edges can lower output and lead to a risk of short circuit. Various treatment methods have been developed to remove the conductivity from wafer edges or to decouple the electrical connection between the top side of the wafer and the conductive edges. These include manual grinding, laser scribing non-conductive grooves, plasma etching, etching by cloth, and masking followed by emersion in etching solution. Compared to previous methods, claim 27 and claims that depend therefrom, drastically reduce the handling steps involved, which further reduces the risk of breakage of the usually thin and fragile silicon wafers. This is accomplished in part by developing a process that permits wafers to lay on a conveyor means for conveying through or over an etching liquid in a controlled manner to selectively expose the conductive edges to an etchant for selective removal of conductivity.

III.

Response to Claim Rejections Under 35 U.S.C. §103 (Obviousness)

A proper obviousness rejection requires consideration of the factual inquiries provided in Graham v. John Deere Co., 38 U.S. 1, 148 USPQ 459 (1966), including: 1) determining the scope and contents of the prior art; 2) ascertaining the differences between the prior art and the claims at issue; 3) resolving the level of ordinary skill in the pertinent art; and 4) considering the objective evidence present in the application indicating obviousness or nonobviousness. Importantly, the differences between the cited references and the claim must be obvious in view of one skilled in the art.

When combining references, it is important to consider the reference as a whole. In Bausch & Lomb, Inc. v. Barnes-Hind/Hydrocurve, Inc., 796 F.2d 443, 230 USPQ 416 (Fed. Cir. 1986), cert. denied, 484 U.S. 823 (1987), the Federal Circuit held that a single line in a prior art reference should not be taken out of context and relied upon with the benefit of hindsight to show obviousness; but instead a reference should be considered as a whole, and portions arguing against or teaching away from the claimed invention must be considered. In addition, an obviousness rejection is not appropriate if substantial

reconstruction or redesign of the prior art reference is necessary to arrive at the invention. In re Ratti, 123 USPQ 349 (C.C.P.A. 1959).

A. Claims 1-26 are Not Obvious Over Hiraishi et al (US 6,506,260)

The examiner rejects claims 1-26 under 35 U.S.C. §103(a) as allegedly being obvious over Hiraishi et al. The examiner argues Hiraishi et al. teach the undersides of silicon wafers being treated in a liquid bath without the top sides previously having been protected or masked. Further, the examiner argues Hiraishi et al. horizontally convey the wafers through a treatment liquid located in the liquid bath. Although the examiner acknowledges the specific treatment compositions enumerated in the claims are not taught by Hiraishi et al., the examiner concludes it would have been obvious to substitute the cleaning compositions taught by Hiraishi et al. with chemical compositions for treatment so as to etch silicon wafers.

On page 6 of the Office Action the examiner further proposes one skilled in the art should be able to control the liquid level so that the wafers which are not to be treated are above the liquid since the level and type of cleaning liquid, position of wafers and oxidizing agents are adjustable parameters which may be optimized for the best results of cleaning or etching.

For clarity the claims are amended to further emphasize that each wafer is treated; however, the top side of each wafer, which is not to be treated, is always positioned above the liquid.

1. With respect to claims 1- 26, it appears the examiner has examined the claims as provided prior to the amendment on September 1, 2009 since the elements set forth in the rejection do not immediately correspond to the claims as amended

As to claims 1-6, 10-15, 17, 19-23 and 26, on page 2, the examiner restates the same argument from the prior office action that Hiraishi et al. treat the underside of silicon wafers without the top side having previously been protected or masked. It seems

this is taken from the prior office action without consideration of the claims as amended. On page 3, the examiner further cites FIG 1a of Hiraishi et al. as showing treatment through the liquid located in the liquid bath without a protective mask.

In the amendment filed September 1, 2009 Applicants amended the claims as follows:

> further wherein ~~without~~ the top sides ~~previously having been proteted or masked~~ of the wafers which are not to be treated are always positioned above the liquid.

Thus, in claims 1 and 10 a mask is not mentioned. It was clarified in the previous Response to Office Action (Sept 1, 2009) that the top sides of wafers which are not to be treated are always positioned above the liquid. This element is not set forth in the rejection. That is, the central theme of the previous response does not appear to be addressed. Instead, it was broadly considered that this is merely an adjustable parameter, which was optimized. However, it is unclear how positioning the top side of the wafer above the liquid is optimization of an adjustable parameter if the central concept of Haraishi et al is to immerse the photovoltaic module in cleaning fluid to remove particles from scribed grooves along the top. For completeness, this is discussed in more detail below.

For still further clarity claims 1 and 10 are amended herein to singular form to recite that the top side of the wafer which is not to be treated is always positioned above the liquid to ensure the claim is examined to mean that each top side of each wafer is always positioned above the liquid.

Now turning back to Hiraishi et al., Hiraishi et al. do not always position the top side of the photovoltaic module above the liquid. Instead, Hiraishi et al. totally immerse the module in the liquid. For example, referring to the Abstract,

> "The cleaning method includes a process for transporting the photovoltaic module immersed in a cleaning fluid, while being kept in a horizontal position with the laminate upward as it is transported, and applying ultrasonic vibration to the cleaning fluid, thereby removing particles in the scribed grooves." (emphasis added)

This is also provided at Col. 3, l. 66 through Col. 4, l. 2, which provides,

"A cleaning method according to the present invention includes a process for transporting a photovoltaic module having scribed grooves and immersed in a cleaning fluid and applying ultrasonic vibration to the cleaning fluid." (emphasis added)

FIG. 1 (reproduced with annotation below) also depicts the photovoltaic module (or substrate) immersed in cleaning solution:

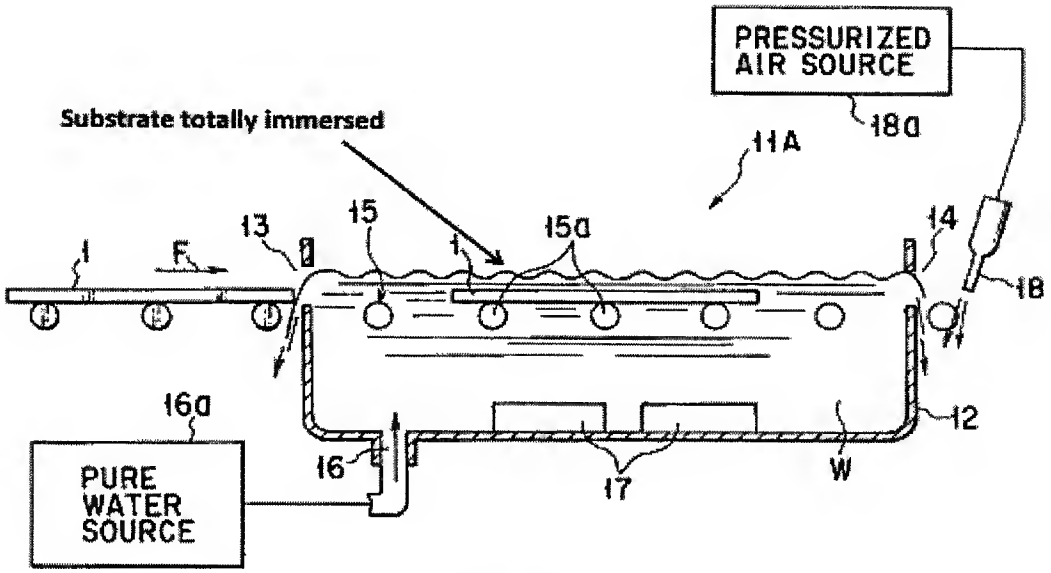


FIG. 1

It is vital that Hiraishi et al. completely immerse the photovoltaic module in the cleaning solution because the purpose for the cleaning step is to remove debris from laser scribed grooves, and the laser scribed grooves are positioned on the top side of the laminate. The need for cleaning the grooves is discussed at Col. 6, ll. 19-41,

"The first electrode layers 3 that individually constitute the photovoltaic cells C are separated from one another by means of grooves 4. The grooves 4 are formed by laser scribing. The second electrode layer 7, which is formed of a metallic film of Ag, Al, or Cr, covers each corresponding semiconductor photovoltaic layer 5. Some of the metallic material that constitutes the second electrode layer 7 fills the grooves 6. The photovoltaic layers 5 and the second electrode layers 7 that constitute the individual photovoltaic cells C are separated electric ally from one

another by means of grooves 8. These grooves 8 are also formed by laser scribing.

As shown in FIG. 7B, particles P, such as swarf, burrs, etc. that are produced by the laser scribing, may be left in the grooves 8, in some cases. The particles P may possibly be produced in the process of laser-scribing grooves 9 that separate a power generating region G from peripheral regions 10, as shown in FIG. 14, for example, as well as the grooves 8. The photovoltaic module 1 with satisfactory electrical insulating properties can be manufactured with high yield by removing the particles P from the scribed grooves." (emphasis added)

For completeness, removal of the particles through immersion of the module in a bath coupled with ultrasonic vibration is discussed at Col. 7, ll. 12-22,

"The photovoltaic module 1 on the conveyor 15 is loaded into the pure water W in the reserver tank 12 through the loading aperture 13. Since the ultrasonic vibration propagates in the pure water W as this is done, the particles P, such as swarf, burrs, etc., left in the scribed grooves 8 and 9 of the module 1 are separated from the module 1. The particles P separated from the module 1 are discharged from the reserver tank 12, along with the pure water W overflowing the reserver tank 12, or sink to the bottom of the tank 12. Therefore, the particles P never adhere again to the photovoltaic module 1." (emphasis added)

Thus, a proper rejection dependent on Hiraishi et al. would require the silicon wafer of the present invention to be immersed in cleaning solution, which it is not. Further, since the purpose of Hiraishi et al. is to clean laser scribed grooves these grooves have not been identified in the claims.

The examiner does argue on page 6, that the type of cleaning liquid, position of wafers, and oxidizing agents are adjustable parameters which are optimized for the best results of cleaning or etching. However, this fails to consider the properties of the silicon wafers themselves in comparison to the photovoltaic module in Hiraishi et al., which is based on a glass substrate.

Hiraishi et al.'s system would not operate with a conventional silicon wafer. As explained in the introduction, consideration of physical properties corresponding to the use of the particular system must also be considered. For instance, when placed in solution, silicon wafers float. Thus, when using the transportation means of Hiraishi et

al., the silicon wafer would lose contact with the transportation means and float away from the desired path. In fact, the operability of Hiraishi et al.'s system is itself dependent on properties such as the surface area to weight ratio being sufficiently low that the substrate or laminate sinks to remain in close contact with the transporting means. This does not pose a problem in Hiraishi et al. because Hiraishi et al. use a glass substrate as the base of the laminate. In other words, in Hiraishi et al.'s system, it is vital that the glass based substrate sink to permit immersion in cleaning fluid and to rest along the transporting means, which permits cleaning of grooves laser scribed on the top side of the laminate. Particular use for glass substrates is discussed at Col. 6, ll. 3-8,

> "A first embodiment of the present invention will now be described with reference to FIG. 1. As shown in FIG. 7A, a thin-film photovoltaic module 1 as an object of cleaning comprises a glass substrate 2 for use as an insulating substrate and photovoltaic cells C that form a laminate L on the substrate 2." (emphasis added)

Therefore, although the examiner considers repositioning the wafer and changing the liquid level falls under ordinary optimization, the inability of a silicon wafer to be used in the system as described in Hiraishi et al supports the finding of non-obviousness. That is, if used in Hiraishi et al., the silicon wafer would lose contact with the transporting means and float away from its desired path thus rendering the method inoperable. Since the system would be inoperable, manipulation of the system to prevent such occurrence would not be encompassed by routine optimization.

For completeness, Hiraishi et al. do suggest the use of silicon within the laminate; however, again the base of the laminate is glass. In other words, it is not a silicon wafer as such. This is provided at Col. 6, ll. 4-13,

> "A first embodiment of the present invention will now be described with reference to FIG. 1. As shown in FIG. 7A, a thin-film photovoltaic module 1 as an object of cleaning comprises a glass substrate 2 for use as an insulating substrate and photovoltaic cells C that form a laminate L on the substrate 2. Each photovoltaic cell C includes a first electrode layer 3, which is formed of a transparent conductive material such as SnO_2, ZnO, or ITO, a semiconductor photovoltaic layer 5 formed of amorphous silicon

or the like, and a second electrode layer 7 formed of a metallic material such as silver (Ag), aluminum (Al), or chromium (Cr)."

The silicon layer in addition to the glass base substrate is demonstrated in the annotated FIG. 7A provided below:

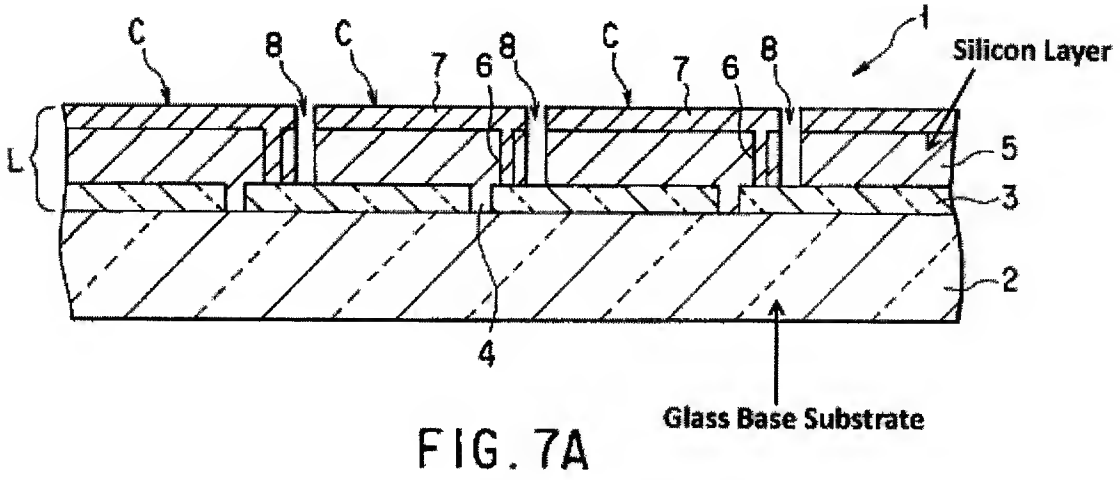


FIG. 7A

Thus, while the laminate includes a silicon layer, the laminate is not a silicon wafer as known in the art. Silicon wafers themselves are discussed in the present application at [0003],

> "First of all, a silicon ingot is cut into slices, also known as wafers, using a wire saw. After they have been cut, the wafers are cleaned in order to remove what is known as a sawing slurry. This is generally followed by a wet-chemical saw damage etch using suitable chemicals, such as in particular lyes, in order to remove the defect-rich layer which results from the cutting process. The wafers are then washed and dried."

Again, as provided in the introduction to the invention, it was expected that any attempt at conveying a silicon wafer through or over liquid would cause the wafer to lose contact with the conveying means and float away from the desired path. This is due in part to the high surface area to low weight ratio of conventional silicon wafers as well as properties of the liquid, such as surface tension. This is in contrast to glass substrates,

which due to their lower surface area to weight ratio, tend to sink to the bottom of a conventional bath. In other words, silicon wafers tend to float when placed in solution; whereas glass based laminate substrates sink.

In this regard, it was surprising to learn that the silicon wafer during treatment can be conveyed through or over the liquid in a controlled and targeted manner without floating apart from their predetermined path.

Thus, while the examiner considers the positioning and relative level of fluid to be a parameter suitable for optimization, since it would be expected that a silicon wafer would lose contact with the conveying means and float away, the skilled artisan would be surprised to find that a silicon wafer can be conveyed through or over liquid located in the bath while always positioning the top side above the liquid.

Further, while the examiner considers the wafer positioning and liquid level to be an adjustable parameter, as devices are miniaturized, the complexity in manipulation of such parameters becomes increasingly difficult. Silicon wafers are quite thin, which requires extensive experimentation to achieve the proper level of fluid. For instance, if a fluid is too low, the underside cannot be wetted. If the liquid level is too high, the silicon wafer may float away. Thus, when approaching the thinness of a silicon wafer even the process itself extends far beyond routine experimentation. This is especially true given the lack of further support by Hiraishi et al.

Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims allowed.

2. **With respect to independent claim 10 and claims that depend therefrom, the examiner has not cited or demonstrated the element of the level of the liquid being contacted by the underside is maintained above the level of the bath surface not being contacted by the underside.**

Claim 10 and claims that depend therefrom recite that the level of the liquid being contacted by the underside is maintained above the level of the bath surface not being contacted by the underside. That is, the area of the liquid contacting the underside is higher than the surrounding bath surface. Hirashi et al. do not provide this element.

As discussed above, Hiraishi et al. totally immerse the laminate in cleaning solution. Thus, in Hiraishi et al. the liquid contacting the underside is lower than the surrounding bath surface. This can be seen in FIG. 1 reproduced above.

For completeness, the examiner proposes altering the position of the substrate and changing the level of the liquid on page 6 of the Office Action. However, the case where liquid being contacted by the underside is maintained above the bath surface has not been specifically addressed. This must extend beyond routine optimization.

Accordingly, Applicant respectfully requests the rejections be withdrawn and the claims allowed.

3. **With respect to claims 7-9, 18, 24 and 25, the examiner proposes reconfiguring the system in Hiraishi to use the cleaning bath as an etching step and altering its liquid level and composition; however, this would include abandonment of the central teaching of Hiraishi et al. and provide a reconfiguration that is not consistent with the Hiraishi et al. design or operation**

The examiner proposes adapting the cleaning step in Hirashi et al. as an etching step for comparison with the claims and on page 6 considers the level and composition of the liquid to be adjustable parameters. While the examiner proposes substituting compositions provided in the cleaning step as taught in Hiraishi et al. to establish an etching step, Hiraishi et al. already provide a technique to solve the same problem addressed by the etching step. In fact, Hiraishi et al.'s solution is the focus of the document. Thus, the examiner's proposal actually abandons the central technical approach taken by Hiraishi et al. Further, the skilled artisan would then be required to reconfigure the washing step to solve the problem addressed by the central technical approach in an entirely different manner.

The purpose of an etching step as well the difference between technical approaches taken by the present invention and Hiraishi et al. are explained in more detail for the convenience of the examiner.

A central problem encountered when applying conductivity to a silicon wafer is that conductivity is often spread beyond the desired surface. That is, conductivity often spreads to the bottom and edges of the wafer. This problem is introduced in the present application at page 2, lines 4-10,

> "One problem with this surface modification is that generally not only the desired surface (top side) but also the opposite surface (underside) and in particular the peripheral edges of the substrate wafers are modified or doped by the treatment, which in subsequent use leads to the risk of short circuits, since the edges are electrically conductive."

Different technical approaches are taken to remove conductivity from select wafer surfaces. For example, one technical approach is to machine grind the wafer edges to remove conductivity. This is summarized at page 2, lines 26-33, which provides,

> "By way of example, the problem of the electrically conductive edges is solved by the edges being ground away mechanically. However, the grinding, like the sawing, can produce defects in the crystal structure, leading to electrical losses. However, the main drawback of this procedure consists in the considerable risk of the sensitive wafers breaking."

Another technical approach for removing electrical conductivity at select regions includes the use of a laser. However, laser treatment of edges has its own technical hurdles. This approach is discussed at page 2, line 35 through page 3, line 9, which provides,

> "Furthermore, it is proposed that the conductive layer which is present on the underside or back surface be interrupted in the outer region or at the edge by the action of a laser beam. However, this edge isolation by means of a laser is not yet an established process and throws up problems in particular with regard to the automation of the process and the throughput which can be achieved. Furthermore, there is a risk that subsequent process steps and the efficiency of, for example, a correspondingly produced cell may be adversely affected by accumulation of combustion products formed during the laser treatment on the wafer surface."

While laser treatment of edges is quite challenging, a laser can be used to along the top side of the wafer to break or decouple an electrical connection. That is, laser treatment of the top side can separate an electrically conductive top portion from an electrically conductive edge. In fact, Hirashi et al. also consider the problem of

electrically conductive edges in the glass laminate substrate and adopt the top side laser treatment approach. Referring to Hiraishi at Col. 2, ll. 47-65,

> "As the electrode layers (3) and (7) of the photovoltaic module (1) are formed, some of the conductive material for the layers (3) and (7) sometimes may get to the end faces and under surfaces of the substrate (2). Although the individual cells C are separated from one another on the substrate (2), in this case, they inevitably conduct to one another by means of the conductive material that adheres to the end faces and under surface of the substrate (2). This results in lowering of the output characteristics of the photovoltaic module (1).
>
> **To solve this problem**, grooves (9) for insulation are formed on the peripheral edge portion of the photovoltaic module (1), as shown in FIG. 14. The grooves (9) serve electrically to separate a power generating region (G), which includes the cells (C) and the groove (8), from its peripheral regions (10). The grooves (9) are formed covering the whole periphery of the module (1) by laser scribing. With use of the grooves (9) formed in this manner, the cells can be prevented from being short-circuited by the conductive material that adheres to the ends faces and under surface of the substrate (2)." (emphasis added)

For completeness an annotated FIG. 14 is reproduced below:

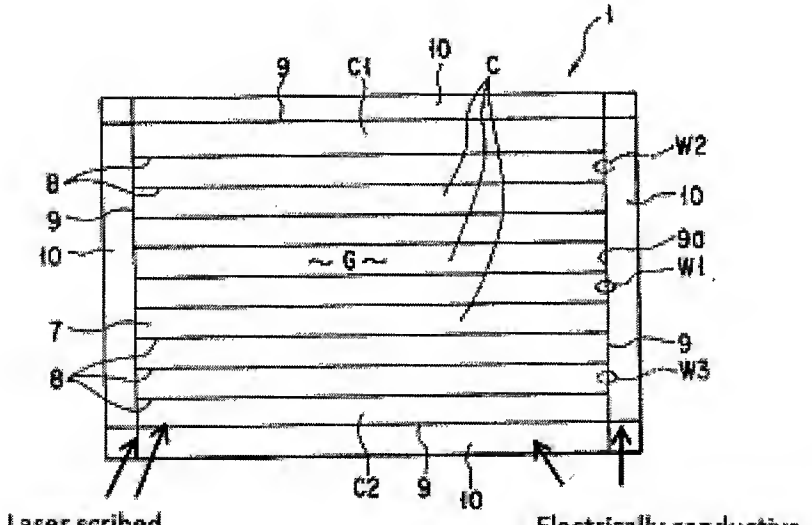


FIG. 14

Since Hiraishi et al. do in fact consider the problem of conductivity beyond the desired surface but instead propose a different technical solution, it would be apparent that the skilled artisan given the teachings of Hiraishi et al. would continue this laser scribing approach for interrupting connections. Again, this approach interrupts the connection between an electrically conductive power portion and an electrically conductive peripheral region or edge.

Further, once adopting the Hiraishi et al. approach there would be no need to provide an etching liquid in the bath because the electrically conductive edges would no longer electrically communicate with the power region.

Again, the etching as set forth in the present invention permits the removal of conductivity from the edges by selective exposure to an etching liquid. Since the present invention provides a significantly different technical approach to solve a similar problem central to Hiraishi et al., the claims are not obvious over Hiraishi et al.

Restated in a different way, instead of removing the conductivity from the edges of the wafer, central to Hiraishi et al. is to form a groove around the top side to decouple the connection between the power source and the electrically conductive peripheral edge. Thus, it is unclear why one skilled in the art would omit the central teaching of Hiraishi et al. to solve the same problem using a different technical approach. That is, the central teaching of Hiraishi et al. is to use a particular step (laser scribing grooves) to address a similar problem set forth by the application (electrical conduction through edges) and thus the skilled artisan would not likely reconfigure a washing step to achieve the same stated result.

B. Claims 1-26 Are Not Obvious Over Wandel et al. (US 6,306,224)

The examiner rejects claims 1-26 under 35 U.S.C. § 103(a) as allegedly being obvious over Wandel et al. The examiner cites Wandel et al. as teaching the treatment of one side of silicon wafers in a liquid bath by lowering the wafers into the liquid bath and horizontally conveying them through the treatment liquid. The examiner cites FIG. 1.

Like the rejection over Hiraishi et al. it appears the examiner did not consider the whether Wandel et al. teach the top side of the wafer which is not to be treated is always

positioned above the liquid. Specifically, Applicants' argument that Wandel et al. teach a rotating disk, which rotates through a bath were not addressed scientifically.

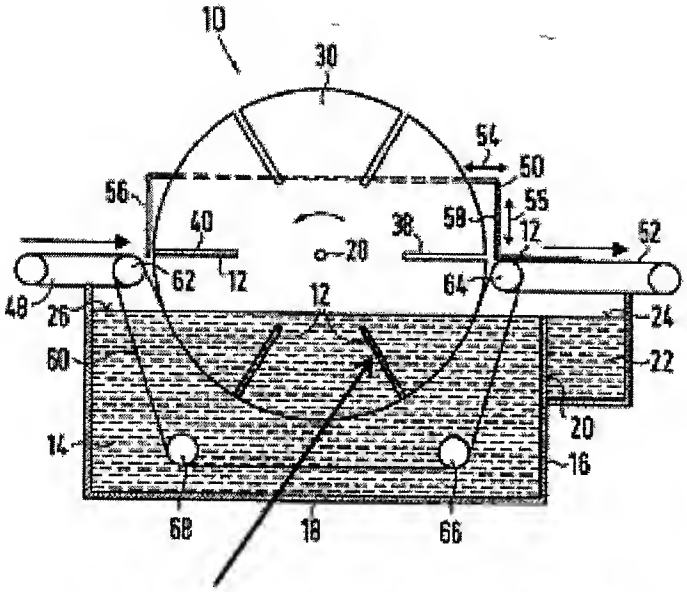
For completeness, while Wandel et al. do appear to provide a horizontal conveyor means flanking a rotating disk, the rotating disk rotates the wafer entirely into the liquid. Further, the rotating disk is central to Wandel et al. as summarized in the Abstract,

> "A process and device for treating sheet objects, especially fragile sheet objects, by rotation through a liquid bath. The objects are disposed in radial slots in a rotating disk, retained therein by a flexible element moving synchronously with the disk, and by a retaining element mounted adjacent the disk and spaced therefrom along its axis of rotation." (emphasis added)

That is, the radial slots retain the wafers permitting their immersion in the liquid bath. Presumably but not explicitly stated, the wafers must be retained for immersion to prevent them from floating away as discussed above. The process is provided in more detail at col. 5, ll.1-9,

> "The conveying device (10), which is designed as a reversing wheel, extends into the bath (16), i.e. into the fluid (14). This means that disk-like elements (30), (32) or (34), (36) (FIG. 2) at a distance from one another are mounted on a shaft (28) and are rotatable jointly about the axis determined by the shaft (28). Extending peripherally from the circumference of the disks (32), (34), (36) are radial slots, numbered (38), (40) as an example. The slots (38), (40) are used as receptacles for the objects (12) to be conveyed through the bath (18) and treated there."

For completeness, FIG. 1 is reproduced below in annotated form to show the treatment of the top side of the wafer during rotation:



Top side of wafer is treated during rotation

In contrast, claims 1-26 provide that the top side of the wafer which is not to be treated is always positioned above the liquid. Since it is clear the top side in Wandel et al. must be positioned within the liquid during treatment of the underside it cannot meet this element.

For completeness, in response to considerations of optimizing a liquid level as set forth in the Office Action at page 6, viewing FIG. 1 above, it is clear the underside cannot contact the liquid while the top side is always above the level of the liquid.

Accordingly, Applicants respectfully request the rejection be withdrawn and the claims allowed.

III.

Additonal Remarks for Newly Added Claims

To expedite allowance, Applicants discuss newly added independent claim 27 and provide additional distinguishing features as compared to Hiraishi et al.

Claim 27 provides a process for wet-chemical treatment of electrically conductive edges of a silicon wafer using a liquid bath, during which treatment the silicon wafer lays on conveyor means, wherein the underside and electrically conductive edges to be treated are conveyed through or over etching liquid located in the liquid bath to remove conductivity from the edges, further wherein the conveyor means are positioned within the liquid bath, further wherein an electrically conductive top side of the wafer which is not to be treated is always positioned above the liquid.

The features of claim 27 are largely discussed with respect to the purpose of the etching step above. Etching the edges removes their conductivity and thus the physical characteristics of the edges themselves, are clearly changed.

Also as discussed above, Hiraishi et al. use a laser scribed groove along the top side of the wafer to prevent electrical connection between the electrically conductive power region and the electrically conductive peripheral region. This is summarized in the passage cited above, "The grooves (9) serve electrically to separate a power generating region (G), which includes the cells (C) and the groove (8), from its peripheral regions (10)." Thus, in addition to the different technical approaches discussed above, the present wafer in comparison to Hiraishi et al.'s substrate have different characteristics, which are further distinguished by the new claim.

Again, in claim 27 electrical conductivity is removed from the edges of the silicon wafer; whereas in Hiraishi et al. the edges retain their electrical conductivity. As such, claim 27 is not obvious over Hiraishi et al.

Accordingly, Applicant also respectfully requests claim 27 be included in the notice of allowance.

IV.
Conclusion

In view of the amendments and remarks above, Applicant respectfully requests all rejections be withdrawn and a notice of allowance be issued for the present application.

Respectfully submitted,

6/2/2010

Date

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